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ABSTRACT (11) 26 Jun 80

The SWIFT algorithm is a new way of computing the discrete Fourier transform (DFT) that can be efficiently implemented in hardware for any range of data rate requirements. It is based on a new decomposition of the discrete Fourier transform and a novel set of implementations of the decomposed equations that leads to hardware that is twice as fast and one-third the size of existing fast Fourier transform (FFT) implementations. Additionally, the algorithm can be applied to any length DFT. This removes the inefficiencies produced by the power of two restriction of the FFT.

1.0 INTRODUCTION

Doppler signal processing hardware based on the fast Fourier transforms (FFT) is the most widely used tool in radar today. In surface-to-surface, surface-to-air, and air-to-air systems it removes ground clutter returns, enhances target signal to noise ratio, and improves target tracking capabilities. It is used in air-to-surface applications for high resolution ground mapping, target tracking and as an aid for navigation systems. The advantages of range-Doppler processing in each of these areas are well understood and for more than ten years the FFT has been the best algorithm for implementing this signal processing technique.

However, today's signal processing requirements are forcing more accurate, faster and smaller Doppler processors. The requirements are growing more rapidly than semiconductor technology, and even though the FFT has been thoroughly refined over the last decade its weaknesses still lead to ineffecient implementations of Doppler processing techniques. Therefore, another approach must be taken in order to meet the rapidly expanding need. The SWIFT algorithm and its various implementations provide a means for meeting these needs by removing the weak points of the FFT and using the strengths of semiconductor technology.

In using the FFT to implement Doppler processing techniques, two major drawbacks that lead to inefficient processors become apparent. They are:

1 The multiplier hardware required between each two point FFT stage slows the transform throughput rate and adds significantly to the power, weight, and volume.

2 FFT flexibility is severely limited by the power of two constraint on transform size. This means that:

a The processor rarely matches the physical problem and thus does not efficiently extract the available target data; and

b The processor must typically be built much larger than the physical problem requires in order to accommodate the power of two constraint. This leads to an inefficient use of hardware power, weight, and volume.

The most rapidly growing technologies in the semiconductor industry today are random access memory (RAM) and programmable read only memory (PROM), because of their wide applicability in all digital designs and the simple, repetitive single bit memory structures of which they are composed.

The SWIFT algorithm relaxes the FFT multiplier constraint by providing a computational structure that permits the efficient use of PROM look up tables for multiplication. Additionally, it removes the FFT flexibility constraint by providing a decomposition technique that allows the efficient implementation of almost any transform length. Together these improvements yield hardware that requires one-third to one-fifth of the power, weight, and volume of a comparable FFT within the same technology.

2.0 SYSTEM APPLICATION OVERVIEW

Terminal guidance sensor studies for advanced ballistic missile defense interceptors have shown that phased array coherent millimeter wave radars form an attractive class of homing sensors for endoatmospheric intercepts in severe dynamic environments (Figure 1). These studies have also shown that a pulse-Doppler radar (Figure 2) with a high pulse repetition frequency burst waveform (Figure 3) is attractive for endoatmospheric intercepts because of terrain and weather clutter. Environmental constraints, scenario dynamics, target characteristics and available transmitter power force the range-Doppler processor to operate at over 400 million arithmetic computations per second to attain the required terminal accuracy.

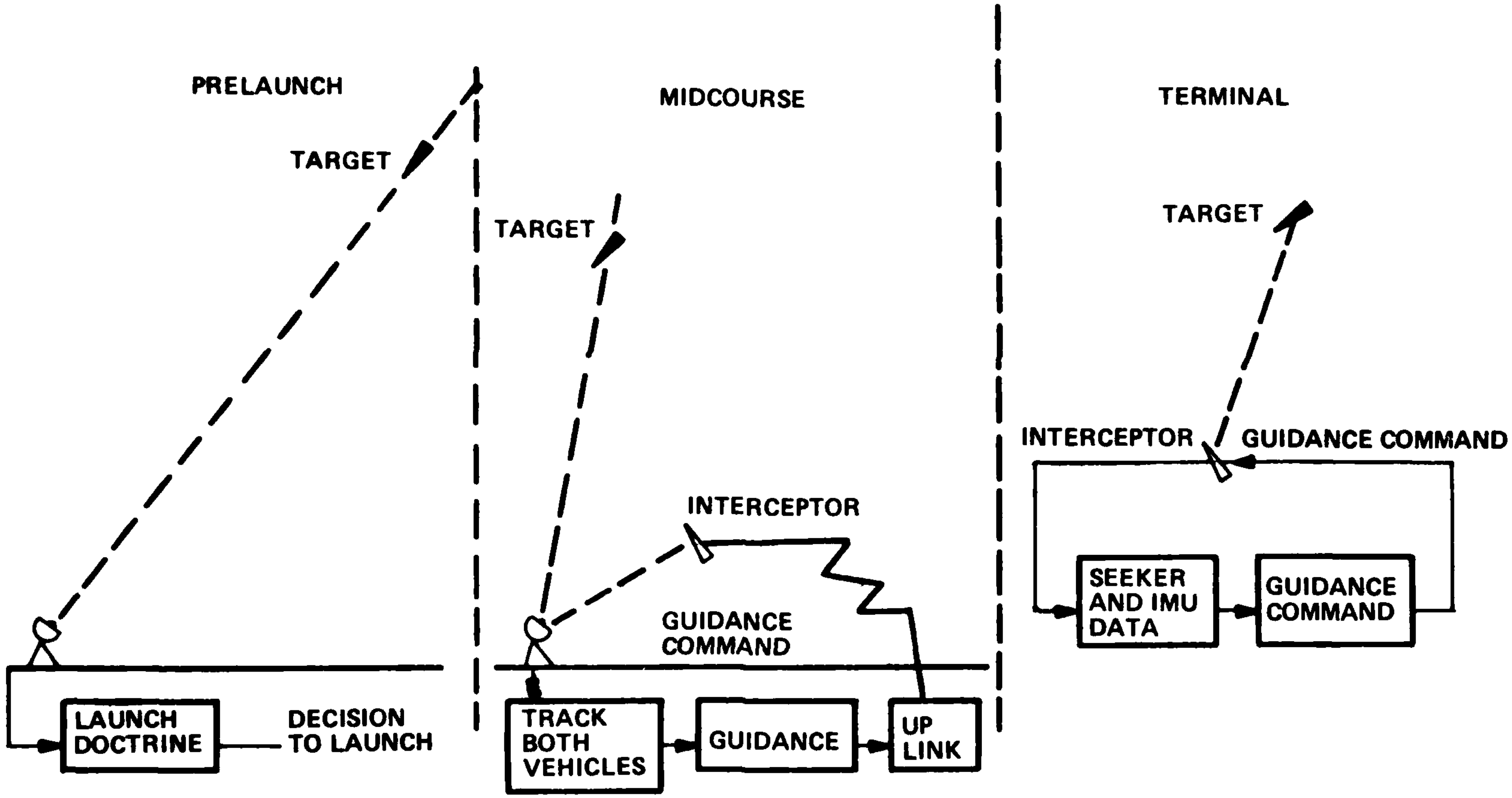

Figure 1. Interceptor Guidance Phases

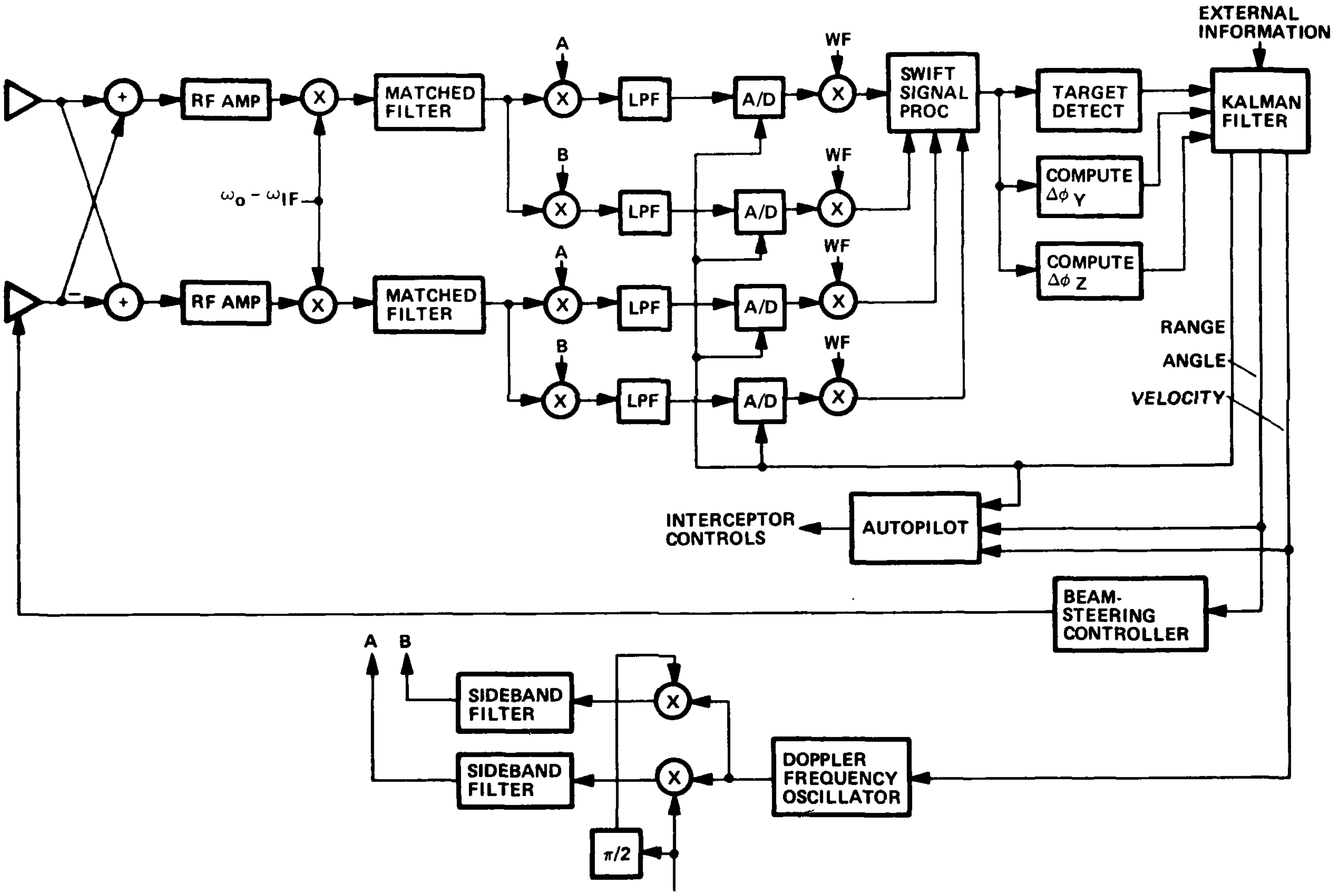

Figure 2. Two Channel Phase-Amplitude Pulse Doppler Radar

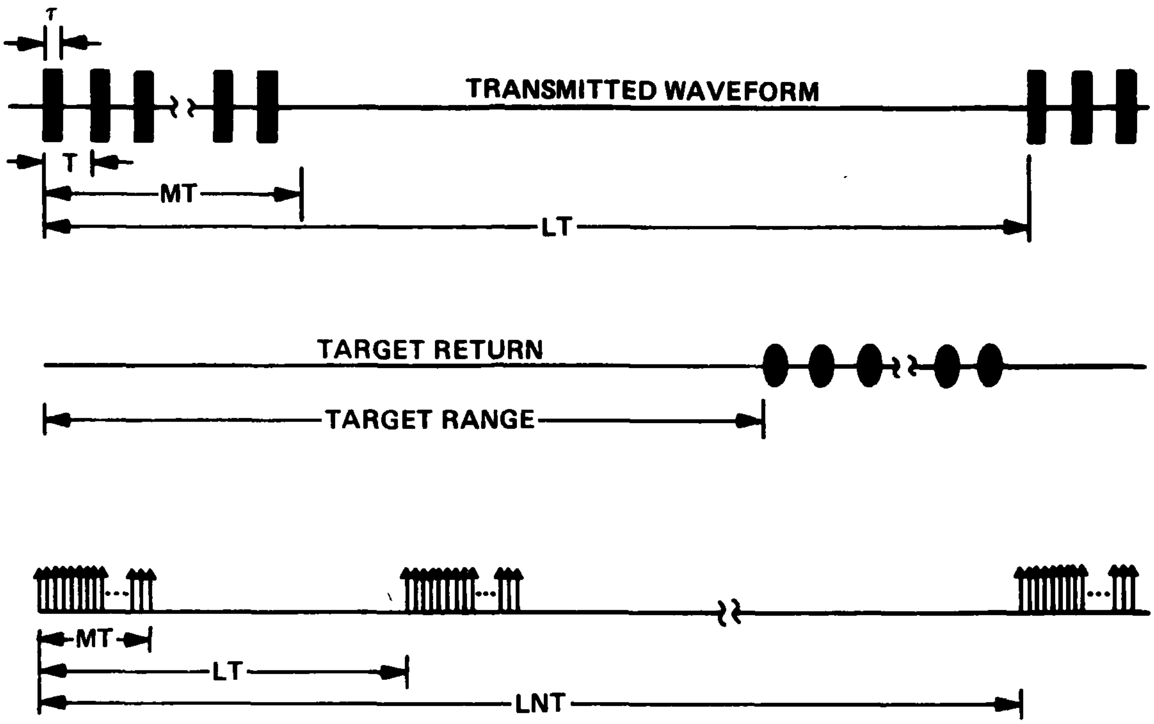

Figure 3. High PRF Pulse Burst Waveform

Interceptor volume constraints have eliminated the FFT or any other existing decomposition of the discrete Fourier transform (DFT) as viable approaches for solving this problem. This has forced a fundamental look at range-Doppler processing to determine how to combine the mathematical properties of the DFT with the best attributes of semiconductor technology to produce a viable solution to the active homing sensor problem. The range-Doppler processor presented in this paper satisfies all of the above criteria and represents an extremely flexible processing structure capable of being used in most low, medium, or high PRF coherent radar systems.

3.0 RANGE-DOPPLER PROCESSING WITH SWIFT

The SWIFT algorithm and its hardware implementations perform the range-Doppler processing task with one-third the hardware of conventional FFT implementations. Additionally, the SWIFT algorithm removes the power of two constraint and thus allows the coherent gain of the processor to be matched to the target and the environment.

The following sections present the key theoretical concepts behind SWIFT and then illustrate these with a description of a 120 point SWIFT hardware demonstrator.

3.1 Theoretical Aspects of SWIFT

The mathematical tools used to obtain the SWIFT algorithm are applied to the DFT in a three step process. First, the N point DFT is decomposed into a sequence of small transform lengths (M_1, M_2, ... M_L) using the standard multidimensional decomposition technique that the FFT algorithm employs when all the small point transforms are 2, 4, or 8 points. Then, by constraining the M_i such that they have no common factors, several facts from ring theory can be used to remove the Twiddle factor multipliers in between the small point transform stages (Figure 4). These techniques are well known; however, the second has rarely been implemented because of the inefficiencies associated with implementing non power of two small point transforms.

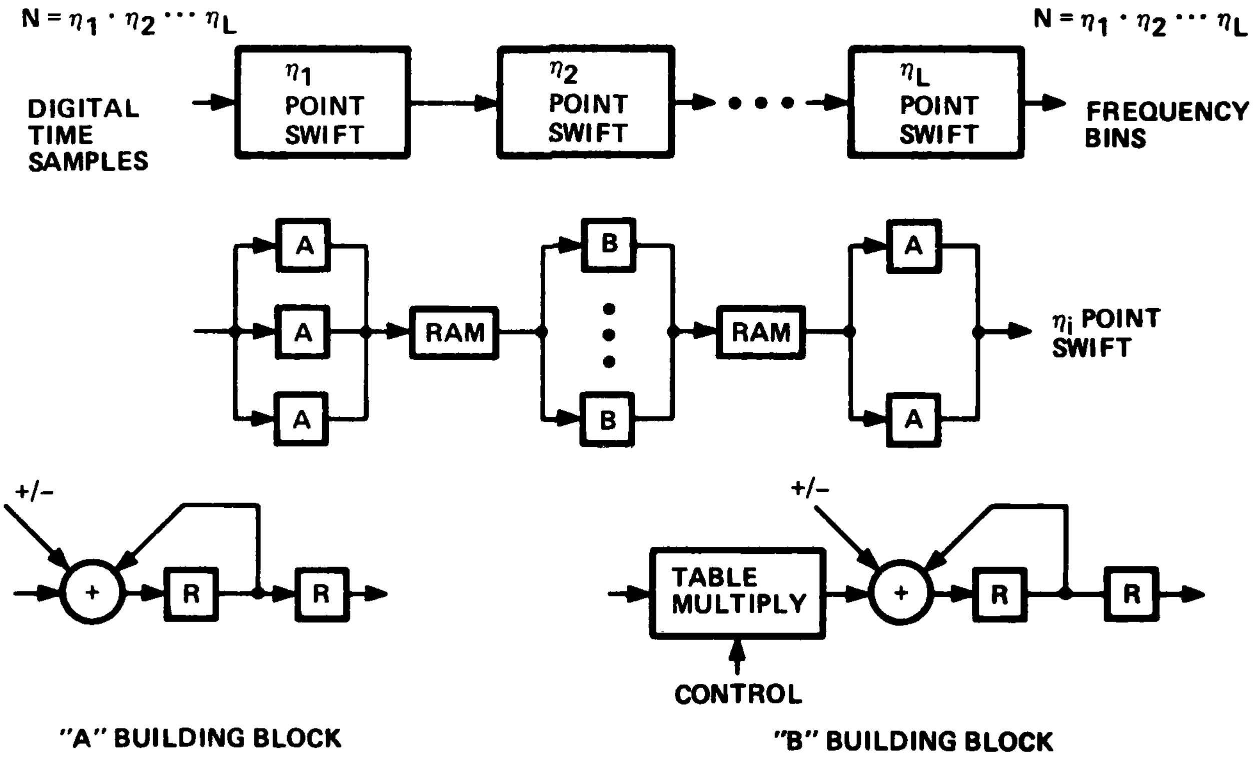

Figure 4. The SWIFT Implementation

The key to the superiority of the SWIFT implementation over the FFT is the SWIFT algorithm for efficiently decomposing the small point transforms for other than powers of two. The SWIFT algorithm is based solely on the concept of complex conjugate symmetry in the DFT computations. Since this symmetry is present for all small point transform lengths and is very simple to manipulate mathematically, it is straightforward to develop the SWIFT algorithm equations for any transform length, M_i.

A 120 point SWIFT hardware demonstrator based on the building block implementation scheme has been designed, built, and tested.

3.2 Proof of Concept Hardware

A 120 point, 12 bit SWIFT processor, Figure 5, has been designed, built and tested using dual inline packages to demonstrate the SWIFT concept and its superiority over FFT approaches. The processor is comprised of a 7 x 11 wire wrapped board for each of the small point SWIFT transform implementations (3, 5, 8) and a board for control hardware and data memory. Table I summarizes the hardware associated with each of these boards.

Each small point transform board is designed for unity coherent gain, multiplication by table look up, and a 7 MHz data rate to illustrate the SWIFT transform concept. A fifth board has been added to the system to generate input signals and display filter output characteristics. The demonstration hardware is capable of displaying the response of all 120 filters to a particular input frequency or the response of a single filter to a variable input frequency. Table II lists the basic characteristics of the proof of concept hardware.

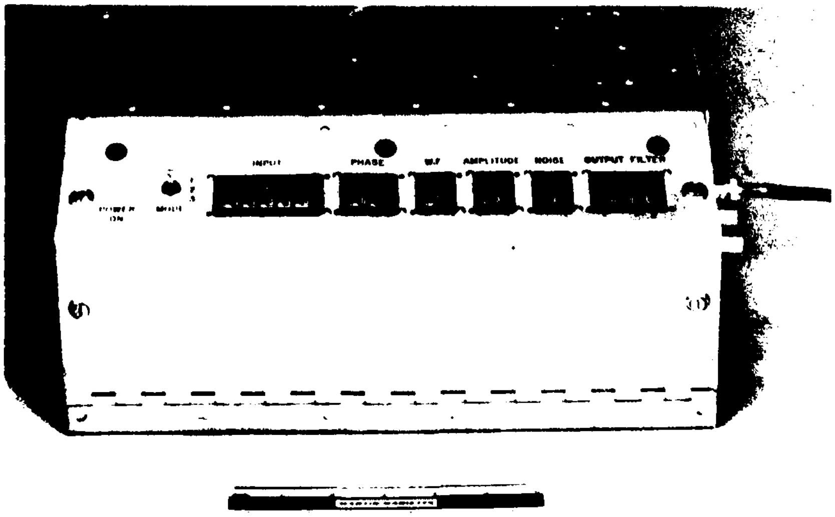

Figure 5. SWIFT 120-Point Processor

TABLE I

Proof of Concept Hardware

Board	Number of Equivalent 16-Pin Chips
3 point SWIFT	79.750
5 point SWIFT	112.125
8 point SWIFT	109.000
Control/memory	104.875
Total	405.750

TABLE II

SWIFT Demonstration Processor Characteristics

Functional	
Transform length	120 complex samples
Coherent gain	Scaled to unity
Dynamic range	12 bits
Input data rate	7 MHz
Conversion time	34 μs
Computation rate	118 million adds per second 39 million multiplies per second
Technology	Available TTL DIP
Area	4-7 x 11 wire wrapped boards
Modes (Variable Amplitude, Phase, Weighting)	
1 Choose input frequency Scan output filters	5,591,040 choices
2 Choose input frequency Choose output filter	670,924,800 choices
3 Sweep input frequency Choose output filter	215,040 choices

4.0 CONCLUSIONS

SWIFT represents a needed step forward in the processing of range-Doppler data in modern radar systems.

The factor of three improvement in the required hardware area provides the system and hardware designers with the capability to:

1. Implement a given range-Doppler signal processor in one-third the volume

2. Process three times the number of range cells in a given hardware volume

3. Compute the Doppler spectrum in much greater detail within a given hardware volume.

The removal of the power of two constraint allows the system designer to design the range-Doppler processor to more closely match the mission and target environment and scenario. It also provides an additional hardware savings when the system requires other than a power of two point Doppler spectrum (i.e., a 300 point SWIFT is less hardware than a 504 point SWIFT).

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